FIG. 1A
PRIOR ART

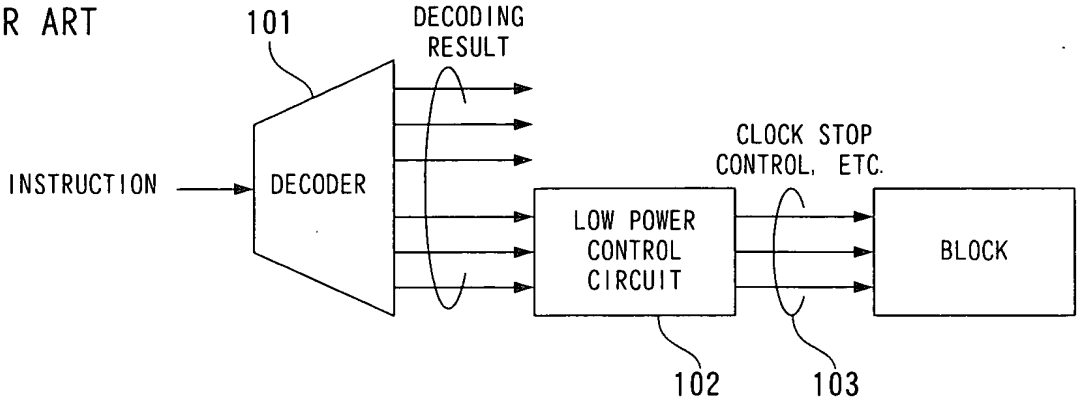

FIG. 1B
PRIOR ART

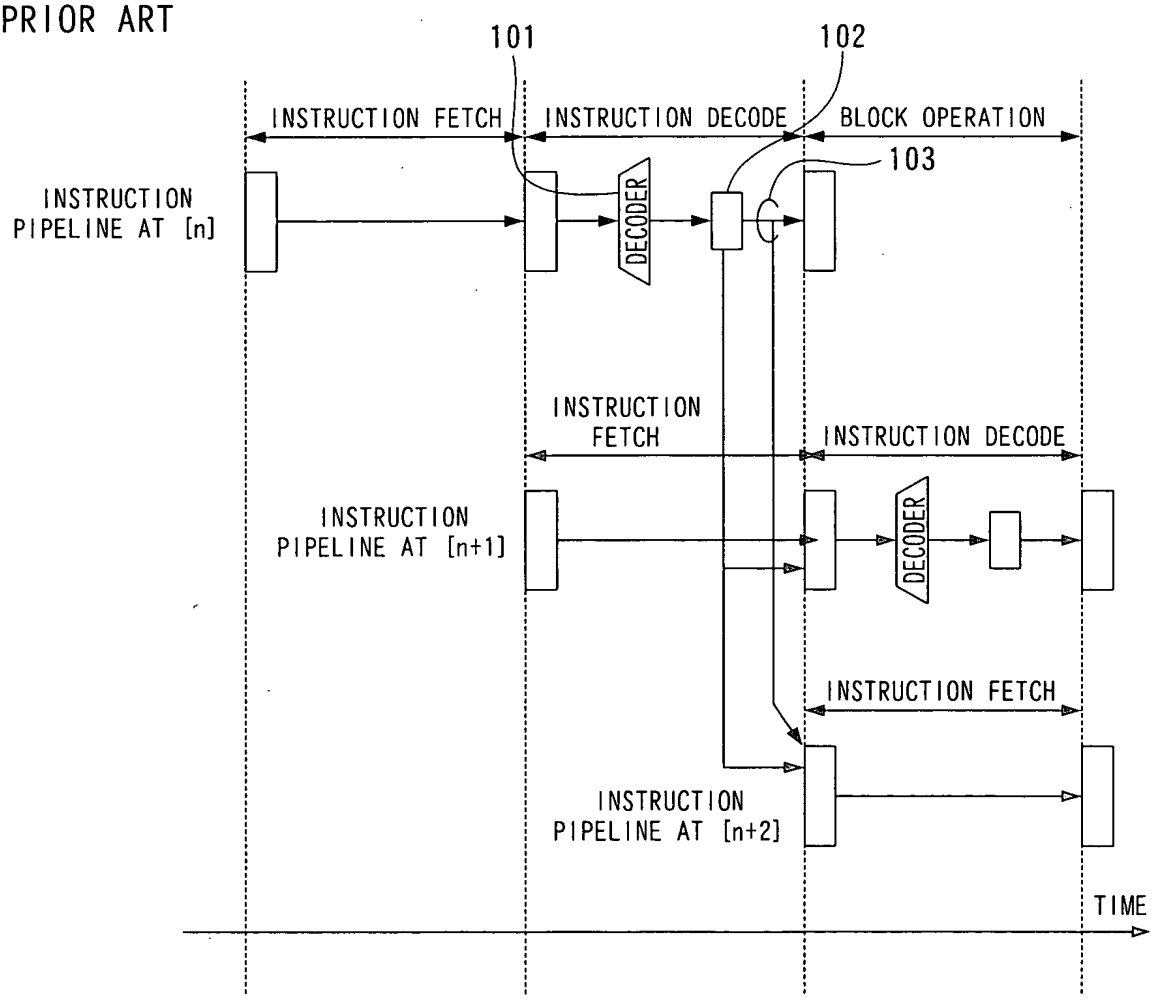

FIG. 2A
PRIOR ART

【NORMAL INSTRUCTION SET】

OPECODE	OPERAND

【LOW POWER INSTRUCTION SET】

LOW POWER CONTROL INFORMATION	OPECODE	OPERAND

FIG. 2B
PRIOR ART

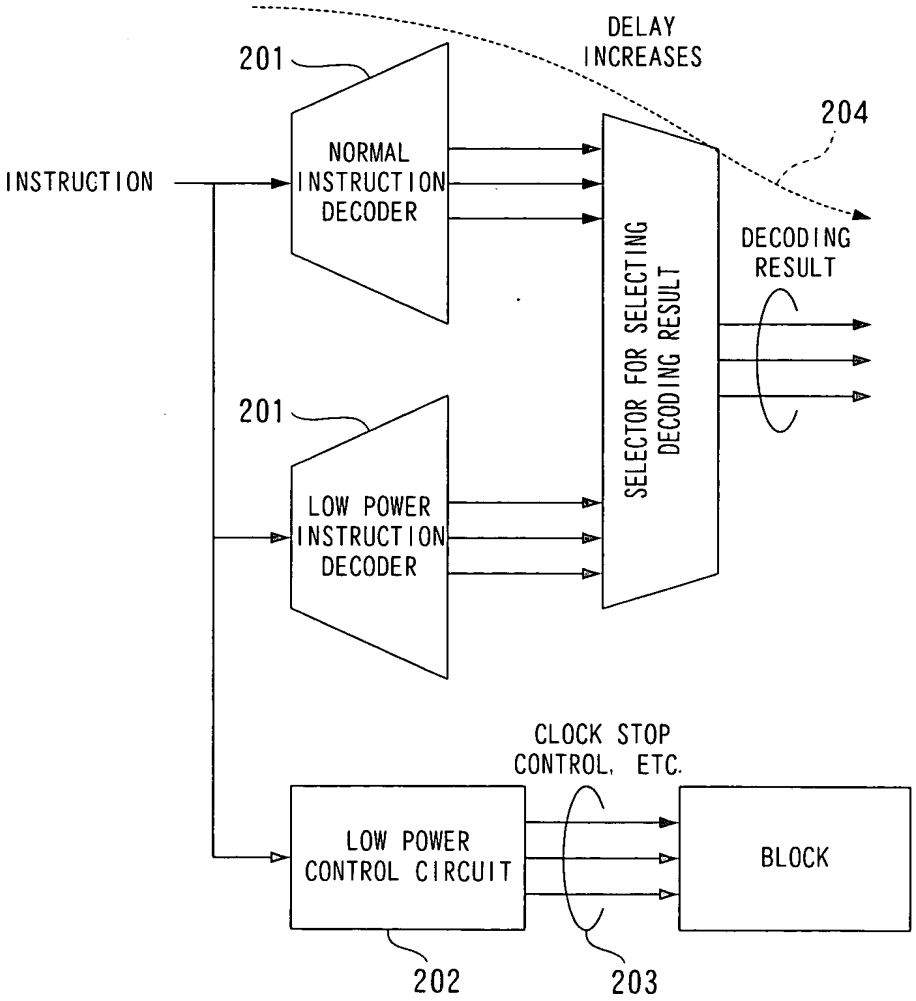

FIG. 3
PRIOR ART

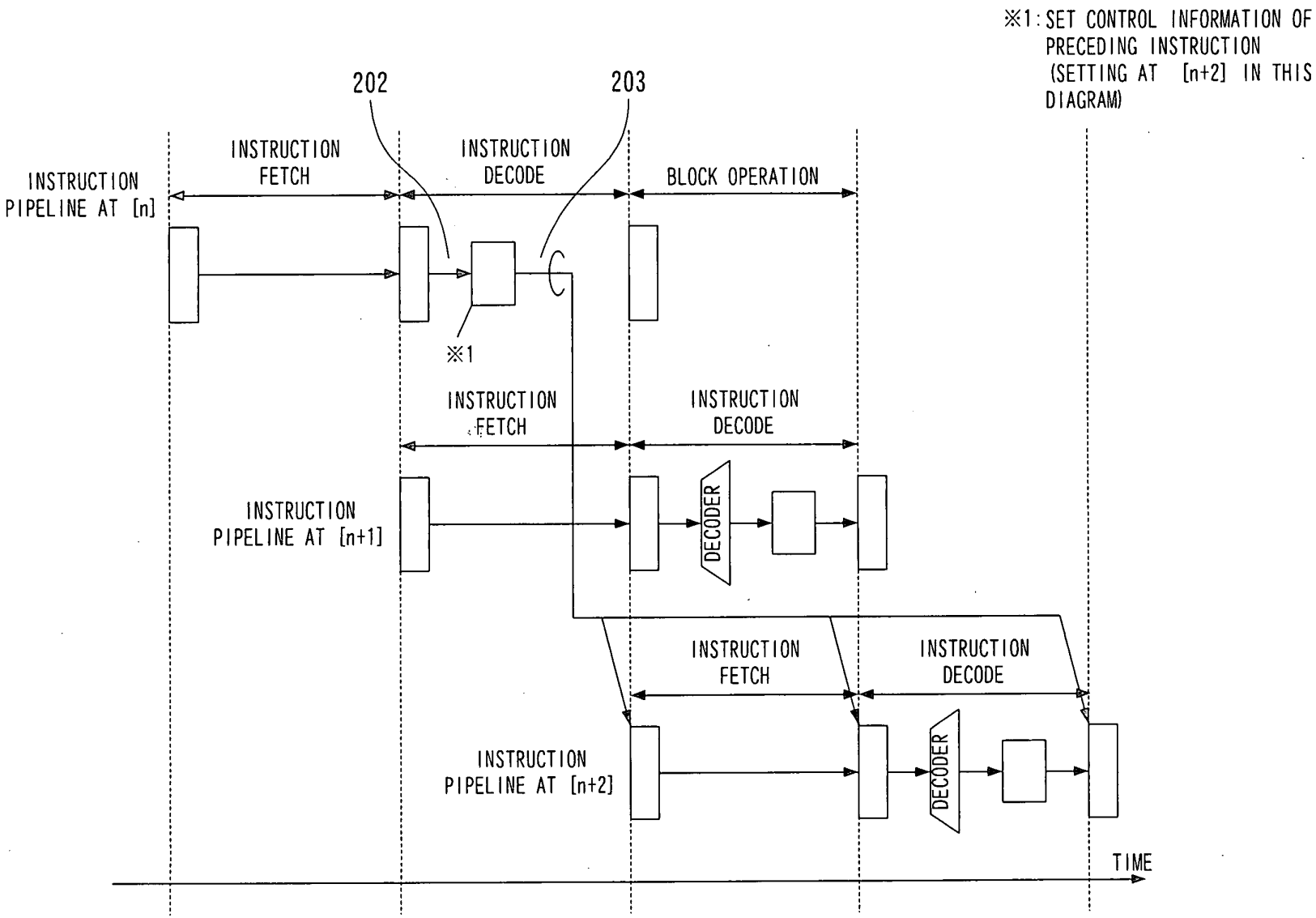

FIG. 4A

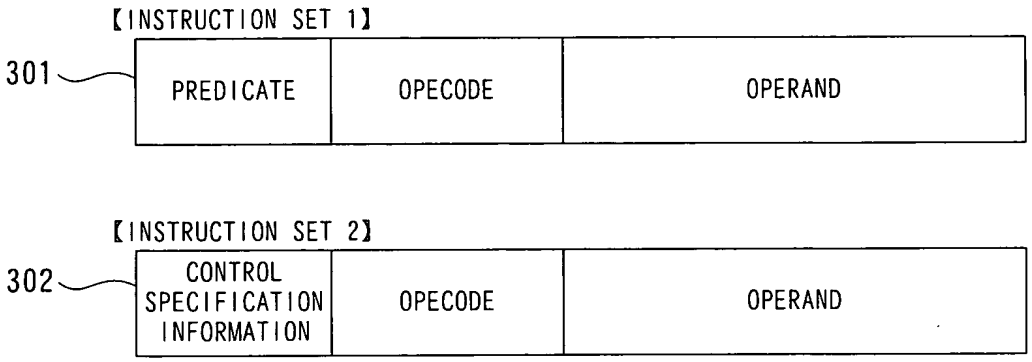
【INSTRUCTION SET 1】
301
PREDICATE
OPECODE
OPERAND
【INSTRUCTION SET 2】
302
CONTROL SPECIFICATION INFORMATION
OPECODE
OPERAND

FIG. 4B

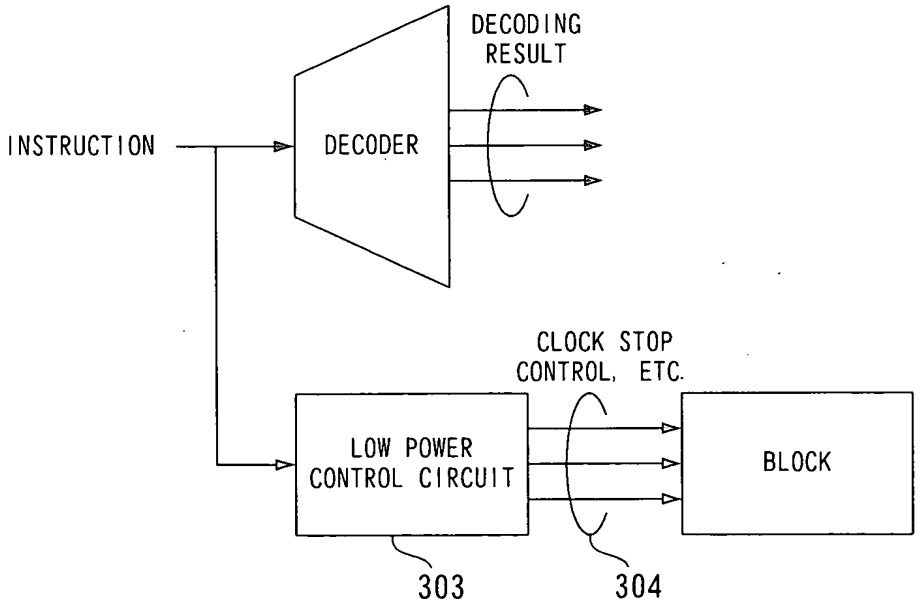
DECODING RESULT
INSTRUCTION
DECODER
CLOCK STOP CONTROL, ETC.
LOW POWER CONTROL CIRCUIT
BLOCK
303
304

FIG. 5

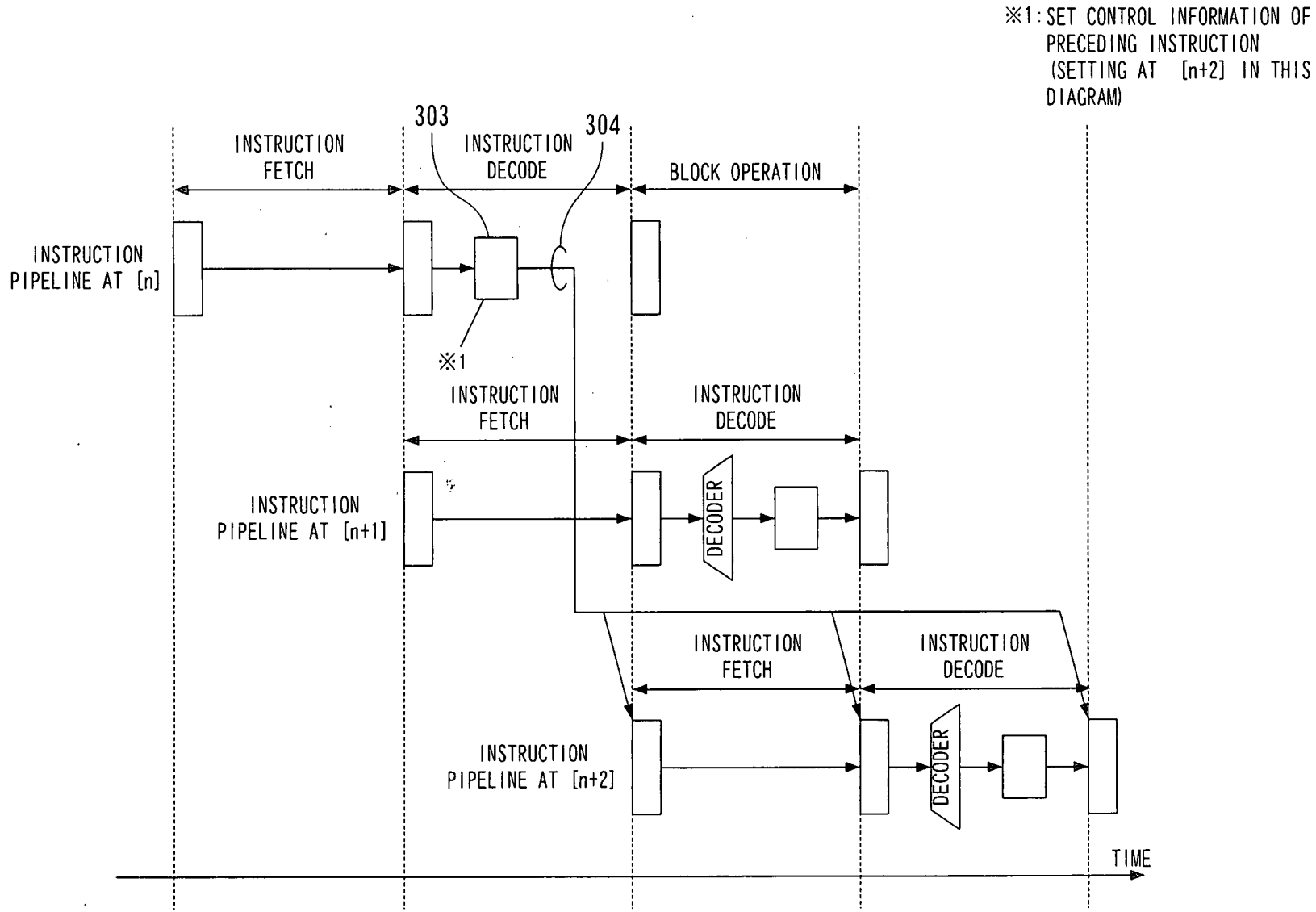
※1: SET CONTROL INFORMATION OF PRECEDING INSTRUCTION (SETTING AT [n+2] IN THIS DIAGRAM)
303
304
INSTRUCTION FETCH
INSTRUCTION DECODE
BLOCK OPERATION
INSTRUCTION PIPELINE AT [n]
※1
INSTRUCTION FETCH
INSTRUCTION DECODE
INSTRUCTION PIPELINE AT [n+1]
DECODER
INSTRUCTION FETCH
INSTRUCTION DECODE
INSTRUCTION PIPELINE AT [n+2]
DECODER
TIME

FIG. 6

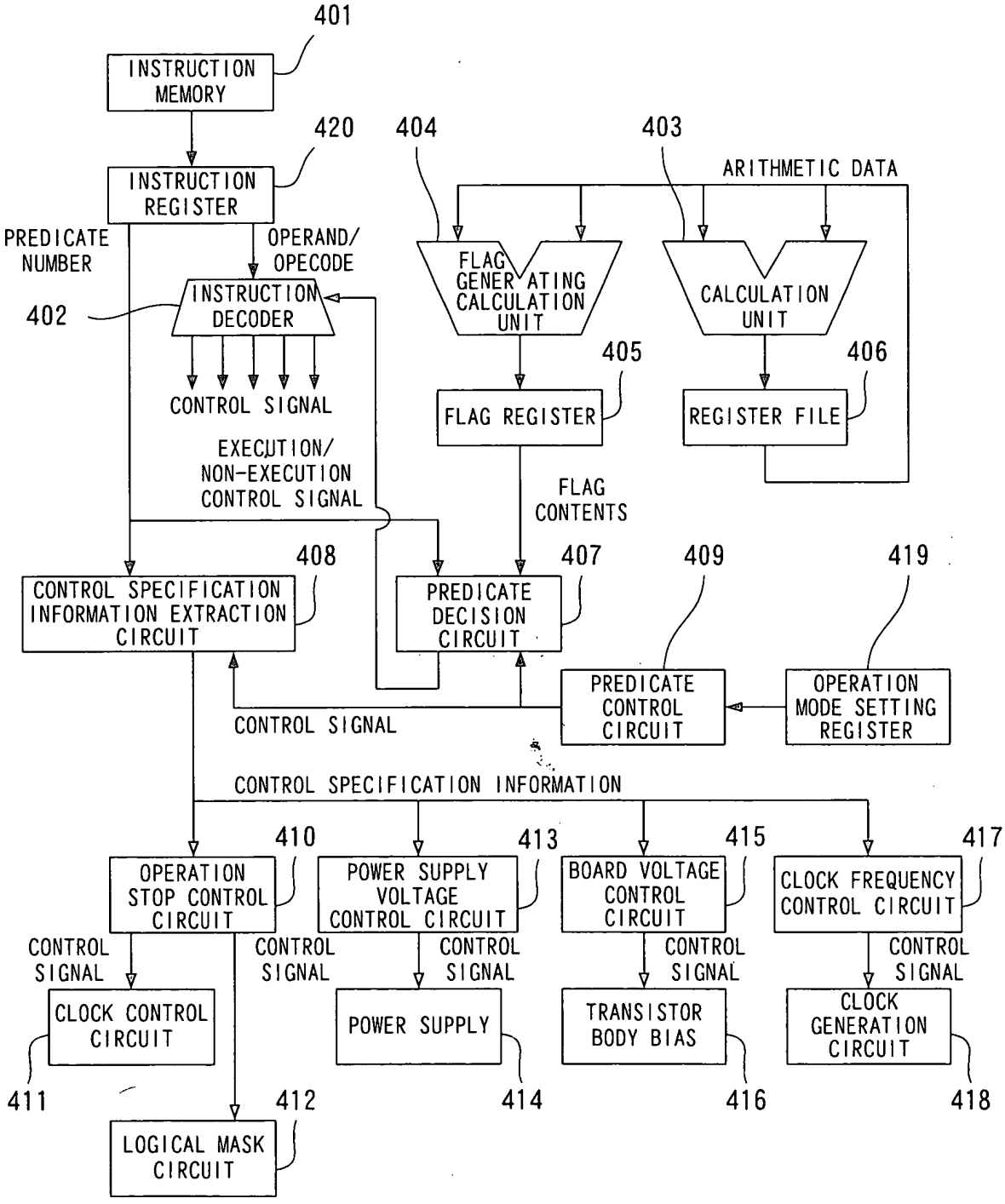
401
INSTRUCTION MEMORY
420
INSTRUCTION REGISTER
404
403
ARITHMETIC DATA
PREDICATE NUMBER
OPERAND/ OPECODE
FLAG GENERATING CALCULATION UNIT
CALCULATION UNIT
402
INSTRUCTION DECODER
405
406
CONTROL SIGNAL
FLAG REGISTER
REGISTER FILE
EXECUTION/ NON-EXECUTION CONTROL SIGNAL
FLAG CONTENTS
408
407
409
419
CONTROL SPECIFICATION INFORMATION EXTRACTION CIRCUIT
PREDICATE DECISION CIRCUIT
PREDICATE CONTROL CIRCUIT
OPERATION MODE SETTING REGISTER
CONTROL SIGNAL
CONTROL SPECIFICATION INFORMATION
410
413
415
417
OPERATION STOP CONTROL CIRCUIT
POWER SUPPLY VOLTAGE CONTROL CIRCUIT
BOARD VOLTAGE CONTROL CIRCUIT
CLOCK FREQUENCY CONTROL CIRCUIT
CONTROL SIGNAL
CONTROL SIGNAL
CONTROL SIGNAL
CONTROL SIGNAL
CONTROL SIGNAL
CLOCK CONTROL CIRCUIT
POWER SUPPLY
TRANSISTOR BODY BIAS
CLOCK GENERATION CIRCUIT
411
414
416
418
412
LOGICAL MASK CIRCUIT

FIG. 7

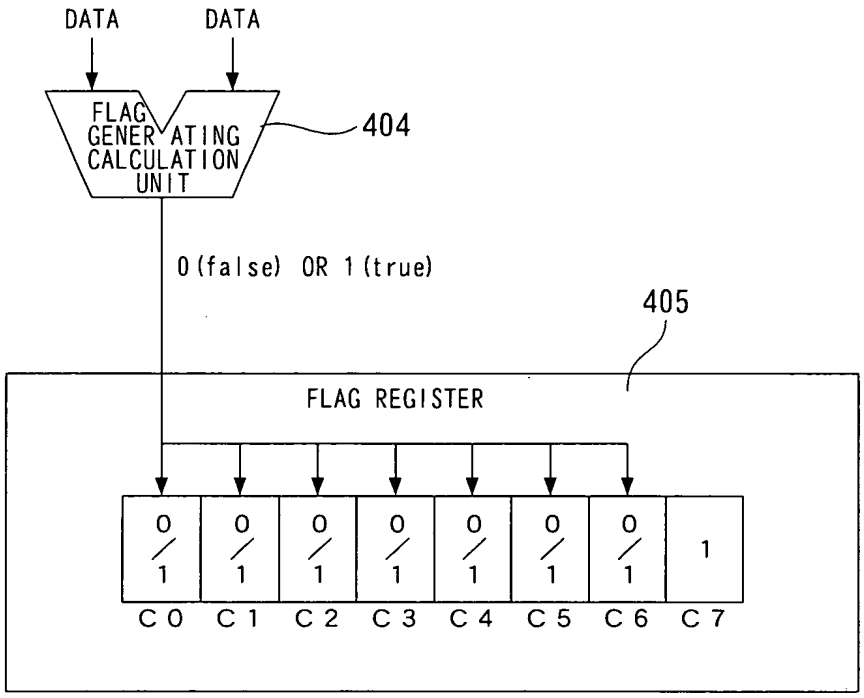
DATA
DATA
FLAG GENERATING CALCULATION UNIT
404
0 (false) OR 1 (true)
405
FLAG REGISTER
0/1
0/1
0/1
0/1
0/1
0/1
0/1
1
C0 C1 C2 C3 C4 C5 C6 C7

FIG. 8

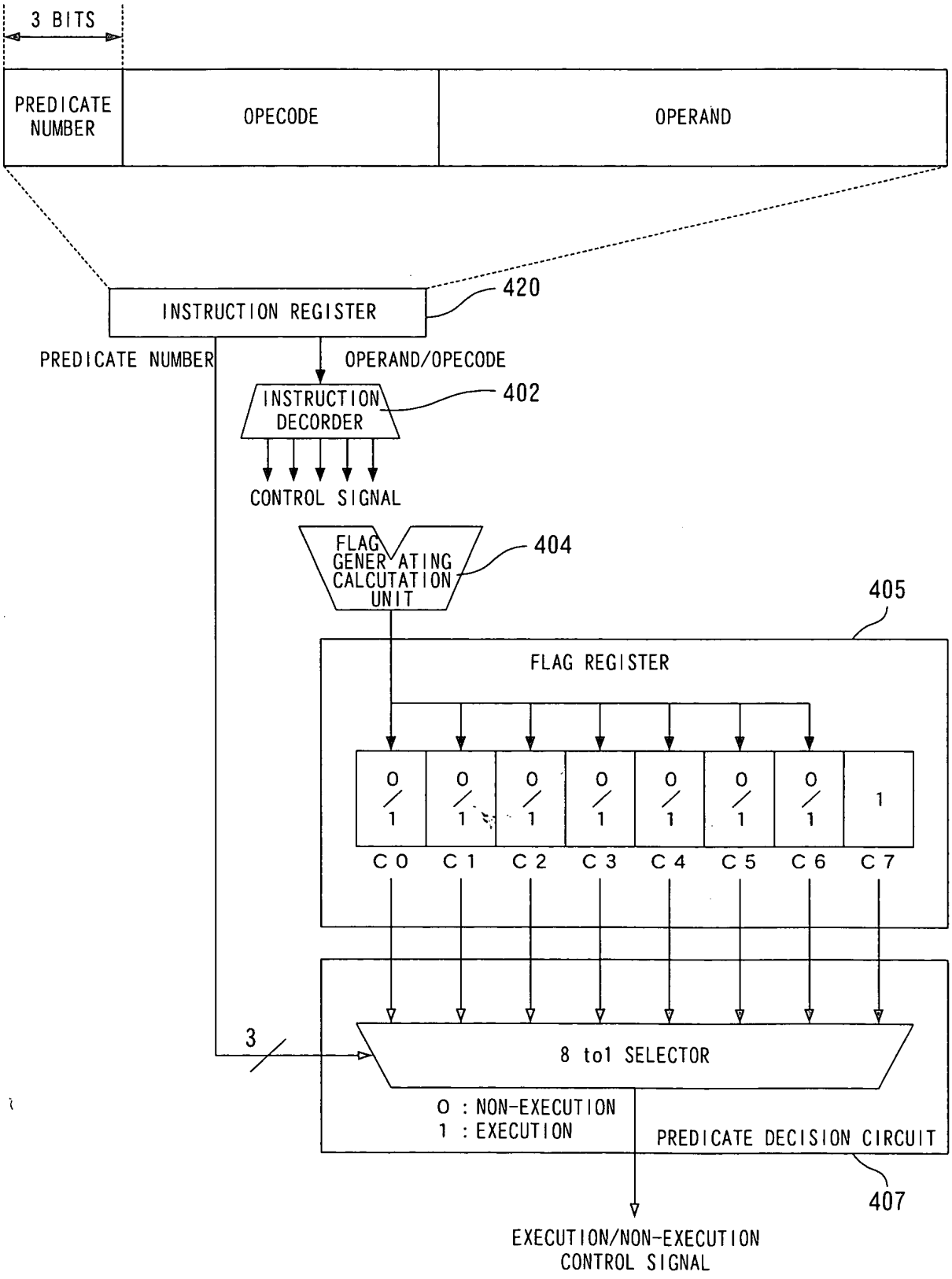
3 BITS
PREDICATE NUMBER
OPECODE
OPERAND
INSTRUCTION REGISTER
420
PREDICATE NUMBER
OPERAND/OPECODE
INSTRUCTION DECORDER
402
CONTROL SIGNAL
FLAG GENERATING CALCUTATION UNIT
404
405
FLAG REGISTER
0/1
1
C0 C1 C2 C3 C4 C5 C6 C7
3
8 to1 SELECTOR
0 : NON-EXECUTION
1 : EXECUTION
PREDICATE DECISION CIRCUIT
407
EXECUTION/NON-EXECUTION CONTROL SIGNAL

FIG. 9

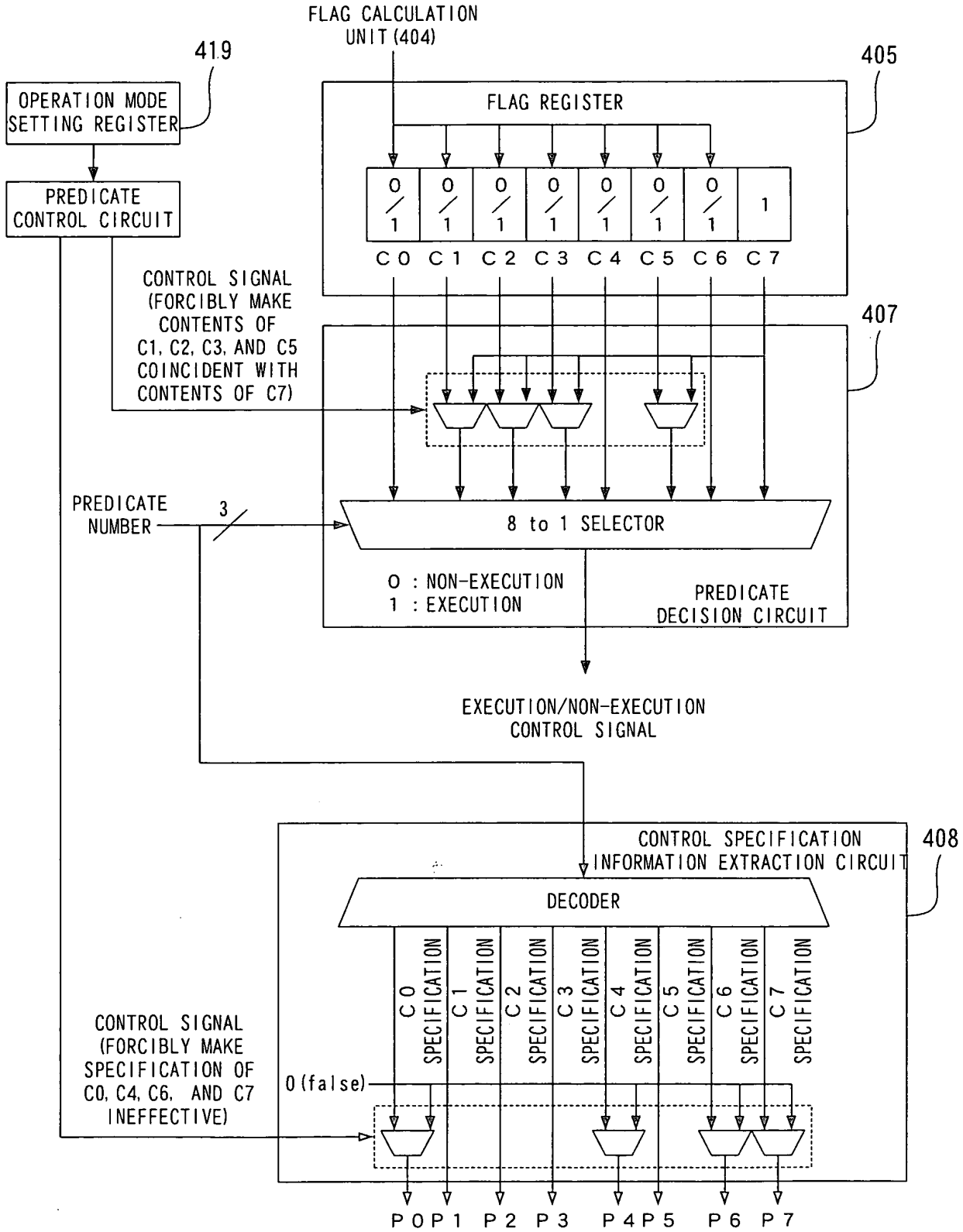
FLAG CALCULATION UNIT (404)
419
405
OPERATION MODE SETTING REGISTER
FLAG REGISTER
PREDICATE CONTROL CIRCUIT
0/1
1
C0 C1 C2 C3 C4 C5 C6 C7
CONTROL SIGNAL (FORCIBLY MAKE CONTENTS OF C1, C2, C3, AND C5 COINCIDENT WITH CONTENTS OF C7)
407
PREDICATE NUMBER
3
8 to 1 SELECTOR
0 : NON-EXECUTION
1 : EXECUTION
PREDICATE DECISION CIRCUIT
EXECUTION/NON-EXECUTION CONTROL SIGNAL
408
CONTROL SPECIFICATION INFORMATION EXTRACTION CIRCUIT
DECODER
C0 SPECIFICATION
C1 SPECIFICATION
C2 SPECIFICATION
C3 SPECIFICATION
C4 SPECIFICATION
C5 SPECIFICATION
C6 SPECIFICATION
C7 SPECIFICATION
CONTROL SIGNAL (FORCIBLY MAKE SPECIFICATION OF C0, C4, C6, AND C7 INEFFECTIVE)
0 (false)
P0 P1 P2 P3 P4 P5 P6 P7

FIG. 10

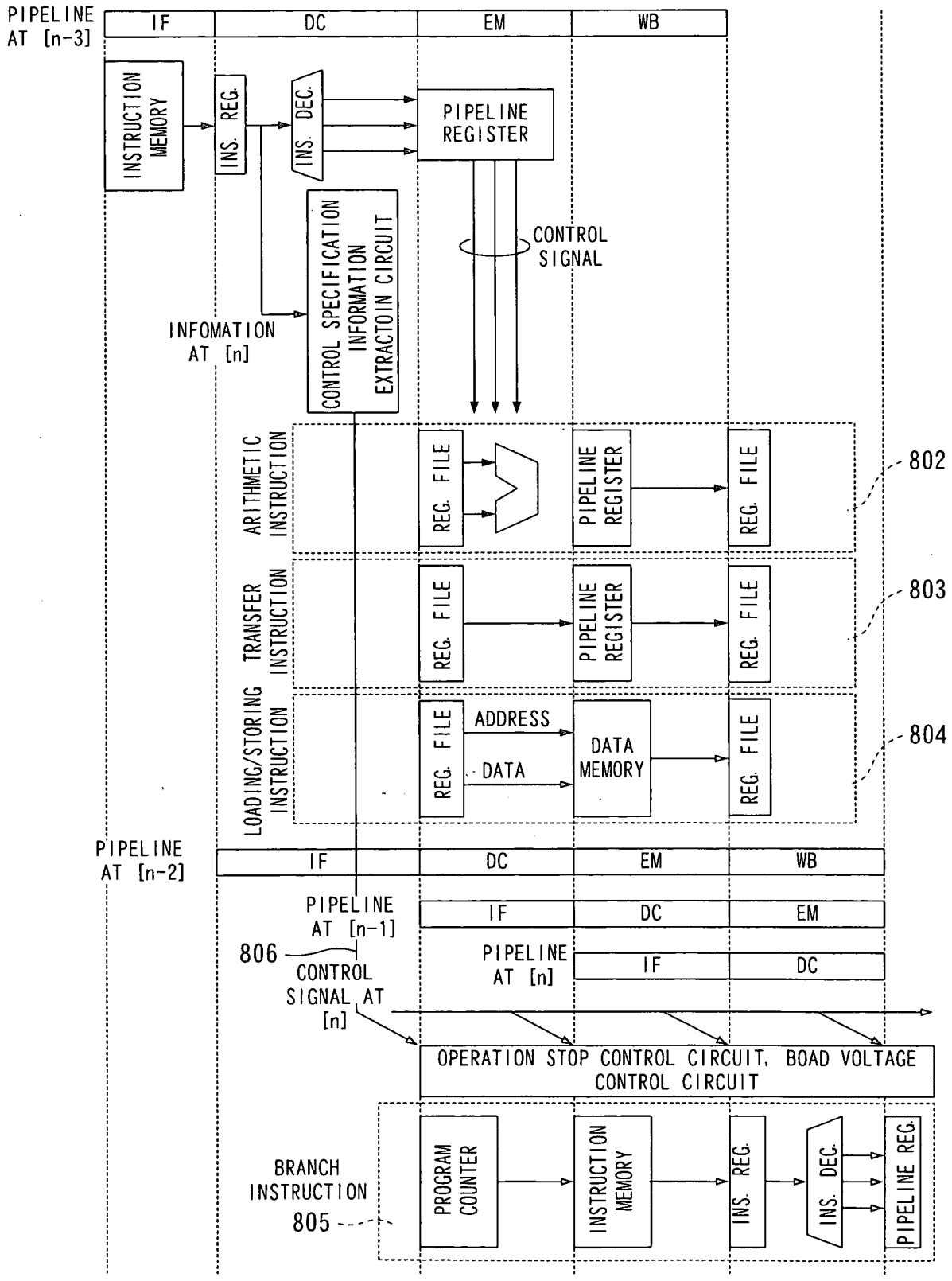
PIPELINE AT [n-3]
IF
DC
EM
WB
INSTRUCTION MEMORY
INS. REG.
INS. DEC.
PIPELINE REGISTER
CONTROL SIGNAL
INFOMATION AT [n]
CONTROL SPECIFICATION INFORMATION EXTRACTOIN CIRCUIT
ARITHMETIC INSTRUCTION
REG. FILE
PIPELINE REGISTER
REG. FILE
802
TRANSFER INSTRUCTION
REG. FILE
PIPELINE REGISTER
REG. FILE
803
LOADING/STORING INSTRUCTION
REG. FILE
ADDRESS
DATA
DATA MEMORY
REG. FILE
804
PIPELINE AT [n-2]
IF
DC
EM
WB
PIPELINE AT [n-1]
IF
DC
EM
806
CONTROL SIGNAL AT [n]
PIPELINE AT [n]
IF
DC
OPERATION STOP CONTROL CIRCUIT, BOAD VOLTAGE CONTROL CIRCUIT
BRANCH INSTRUCTION
805
PROGRAM COUNTER
INSTRUCTION MEMORY
INS. REG.
INS. DEC.
PIPELINE REG.

FIG. 11

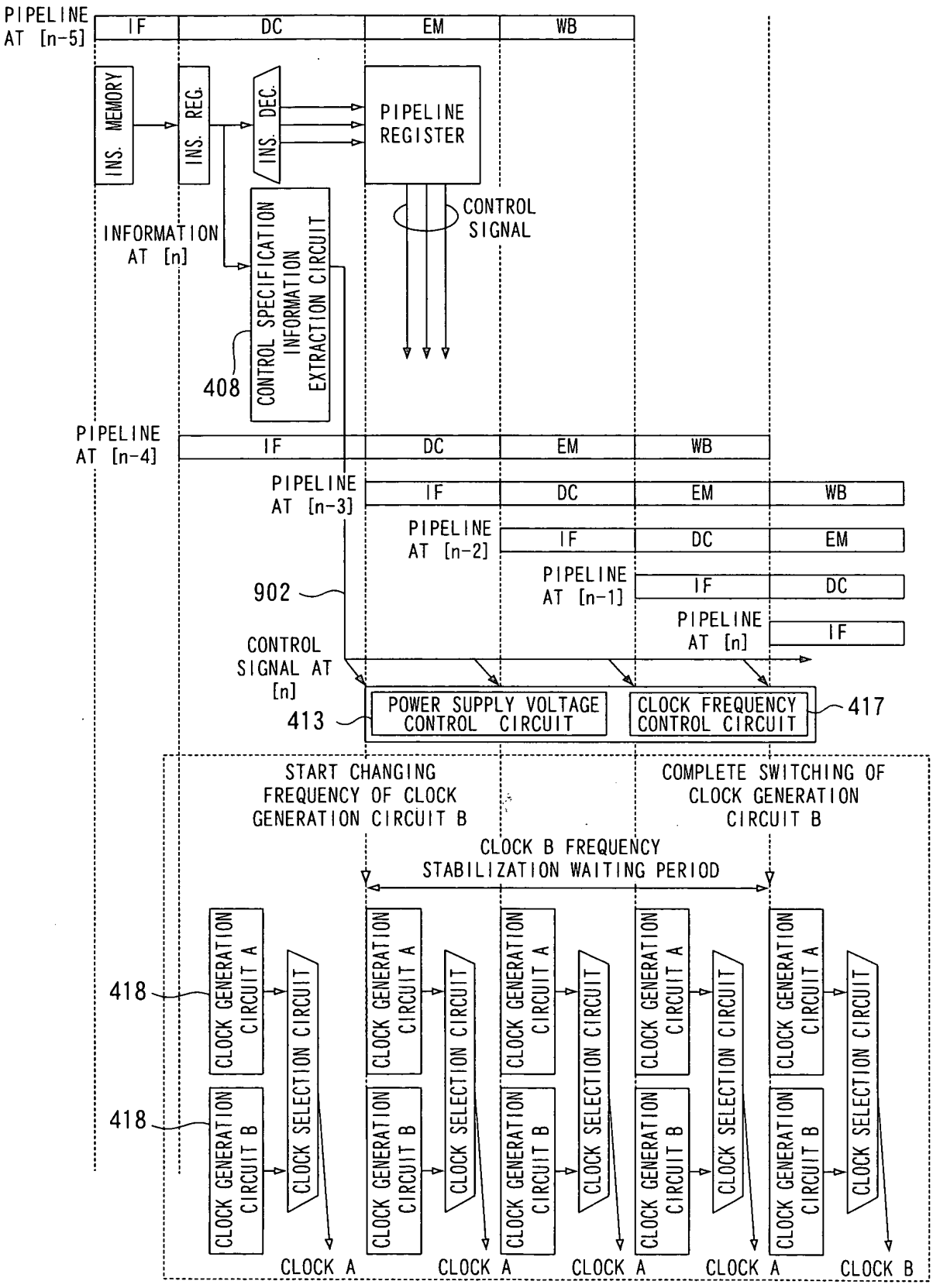
PIPELINE AT [n-5]
IF
DC
EM
WB
INS. MEMORY
INS. REG.
INS. DEC.
PIPELINE REGISTER
CONTROL SIGNAL
INFORMATION AT [n]
CONTROL SPECIFICATION INFORMATION EXTRACTION CIRCUIT
408
PIPELINE AT [n-4]
PIPELINE AT [n-3]
PIPELINE AT [n-2]
PIPELINE AT [n-1]
PIPELINE AT [n]
902
CONTROL SIGNAL AT [n]
POWER SUPPLY VOLTAGE CONTROL CIRCUIT
CLOCK FREQUENCY CONTROL CIRCUIT
413
417
START CHANGING FREQUENCY OF CLOCK GENERATION CIRCUIT B
COMPLETE SWITCHING OF CLOCK GENERATION CIRCUIT B
CLOCK B FREQUENCY STABILIZATION WAITING PERIOD
418
418
CLOCK GENERATION CIRCUIT A
CLOCK GENERATION CIRCUIT B
CLOCK SELECTION CIRCUIT
CLOCK A
CLOCK A
CLOCK A
CLOCK A
CLOCK B

FIG. 12

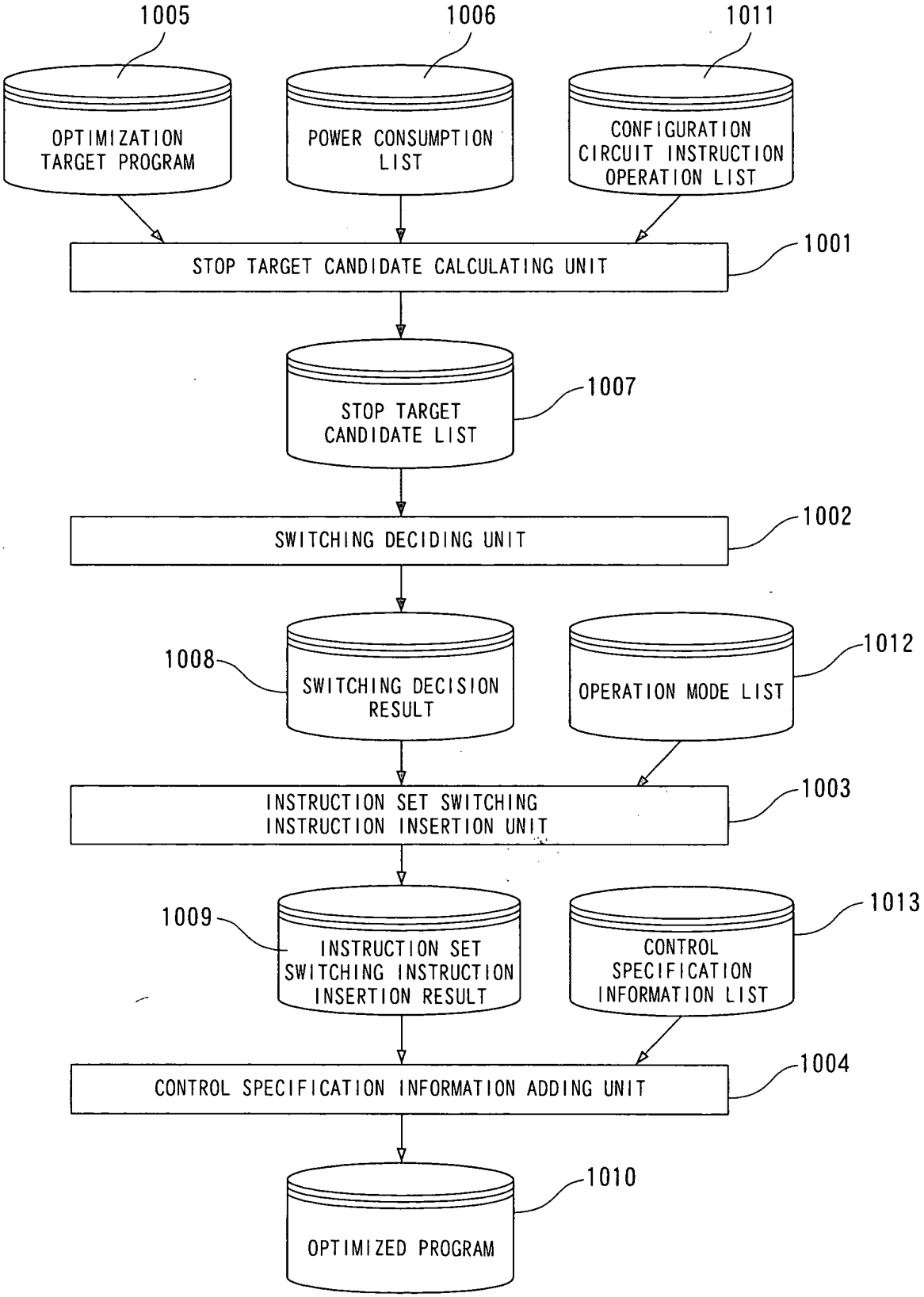
1005
1006
1011
OPTIMIZATION TARGET PROGRAM
POWER CONSUMPTION LIST
CONFIGURATION CIRCUIT INSTRUCTION OPERATION LIST
STOP TARGET CANDIDATE CALCULATING UNIT
1001
STOP TARGET CANDIDATE LIST
1007
SWITCHING DECIDING UNIT
1002
1008
SWITCHING DECISION RESULT
OPERATION MODE LIST
1012
INSTRUCTION SET SWITCHING INSTRUCTION INSERTION UNIT
1003
1009
INSTRUCTION SET SWITCHING INSTRUCTION INSERTION RESULT
CONTROL SPECIFICATION INFORMATION LIST
1013
CONTROL SPECIFICATION INFORMATION ADDING UNIT
1004
OPTIMIZED PROGRAM
1010

FIG. 13

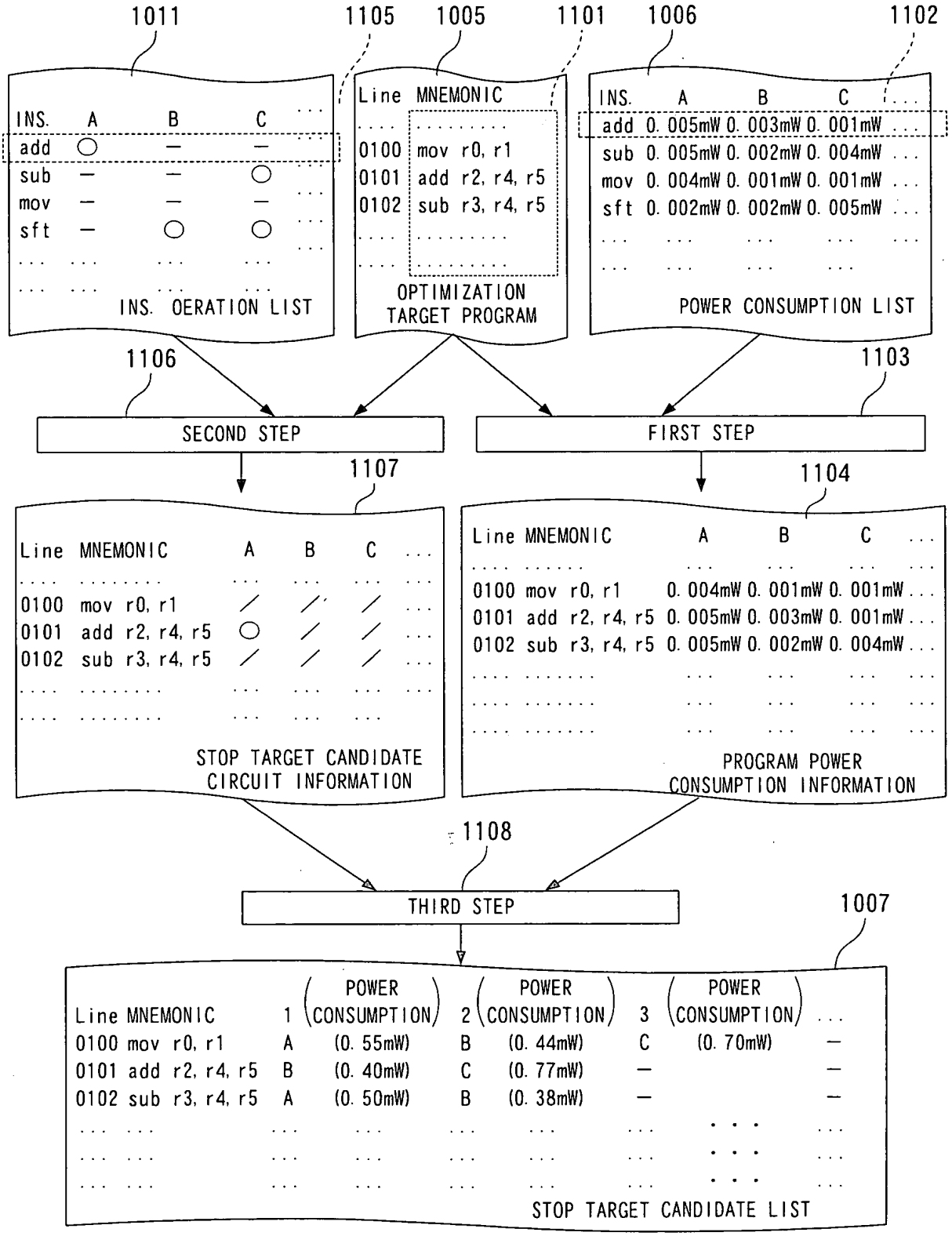
1011
1105
1005
1101
1006
1102
INS. A B C ...
add ○ — — ...
sub — — ○ ...
mov — — — ...
sft — ○ ○ ...
INS. OERATION LIST
Line MNEMONIC
0100 mov r0, r1
0101 add r2, r4, r5
0102 sub r3, r4, r5
OPTIMIZATION TARGET PROGRAM
INS. A B C ...
add 0. 005mW 0. 003mW 0. 001mW ...
sub 0. 005mW 0. 002mW 0. 004mW ...
mov 0. 004mW 0. 001mW 0. 001mW ...
sft 0. 002mW 0. 002mW 0. 005mW ...
POWER CONSUMPTION LIST
1106
1103
SECOND STEP
FIRST STEP
1107
1104
Line MNEMONIC A B C ...
0100 mov r0, r1 ／ ／ ／ ...
0101 add r2, r4, r5 ○ ／ ／ ...
0102 sub r3, r4, r5 ／ ／ ／ ...
STOP TARGET CANDIDATE CIRCUIT INFORMATION
Line MNEMONIC A B C ...
0100 mov r0, r1 0. 004mW 0. 001mW 0. 001mW ...
0101 add r2, r4, r5 0. 005mW 0. 003mW 0. 001mW ...
0102 sub r3, r4, r5 0. 005mW 0. 002mW 0. 004mW ...
PROGRAM POWER CONSUMPTION INFORMATION
1108
THIRD STEP
1007
Line MNEMONIC 1 (POWER CONSUMPTION) 2 (POWER CONSUMPTION) 3 (POWER CONSUMPTION) ...
0100 mov r0, r1 A (0. 55mW) B (0. 44mW) C (0. 70mW) —
0101 add r2, r4, r5 B (0. 40mW) C (0. 77mW) — —
0102 sub r3, r4, r5 A (0. 50mW) B (0. 38mW) — —
STOP TARGET CANDIDATE LIST

FIG. 14

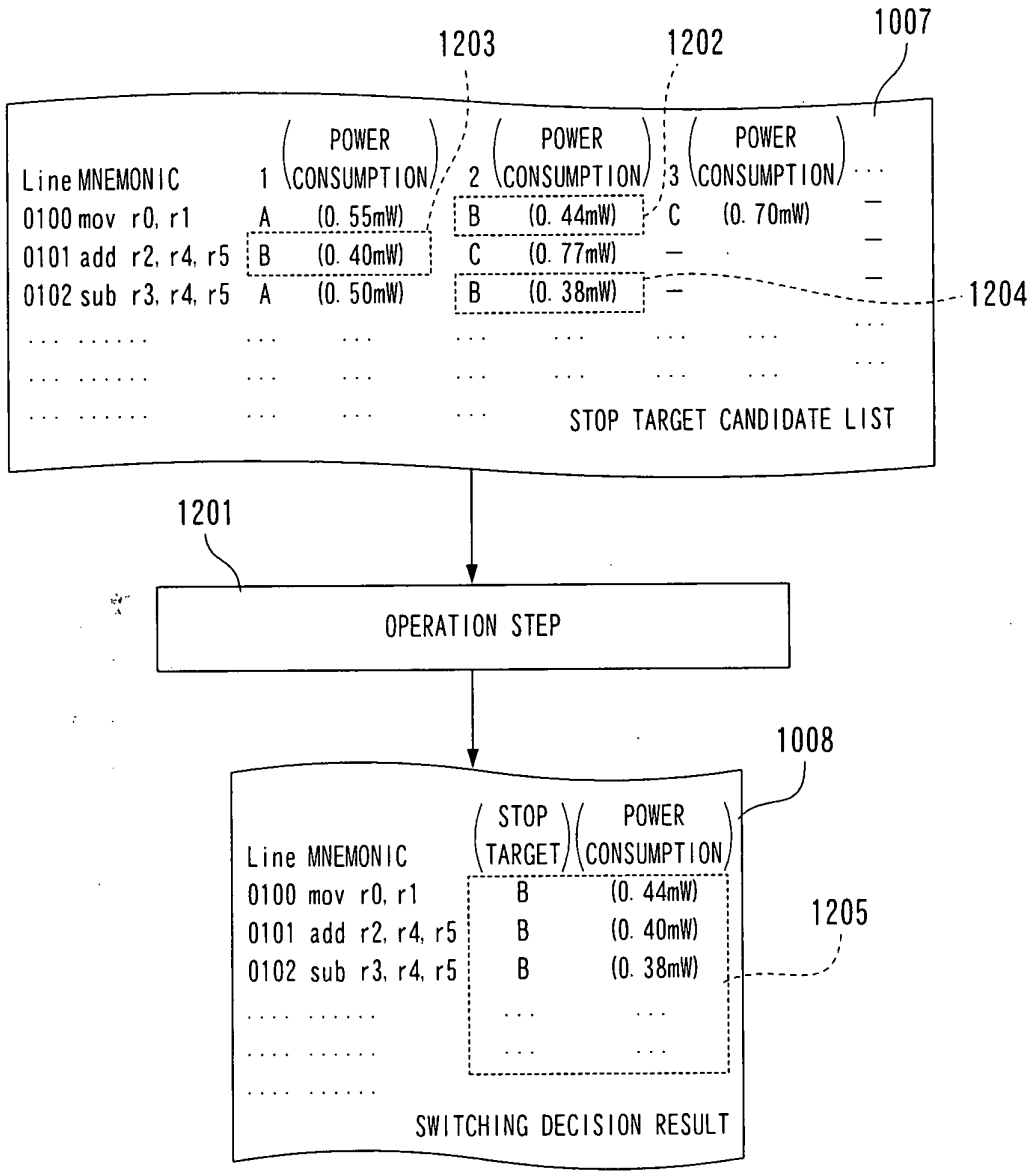
1203
1202
1007
Line MNEMONIC
1 POWER CONSUMPTION
2 POWER CONSUMPTION
3 POWER CONSUMPTION
0100 mov r0, r1
A (0.55mW)
B (0.44mW)
C (0.70mW)
0101 add r2, r4, r5
B (0.40mW)
C (0.77mW)
0102 sub r3, r4, r5
A (0.50mW)
B (0.38mW)
1204
STOP TARGET CANDIDATE LIST
1201
OPERATION STEP
1008
Line MNEMONIC
STOP TARGET
POWER CONSUMPTION
0100 mov r0, r1
B (0.44mW)
0101 add r2, r4, r5
B (0.40mW)
0102 sub r3, r4, r5
B (0.38mW)
1205
SWITCHING DECISION RESULT

FIG. 15

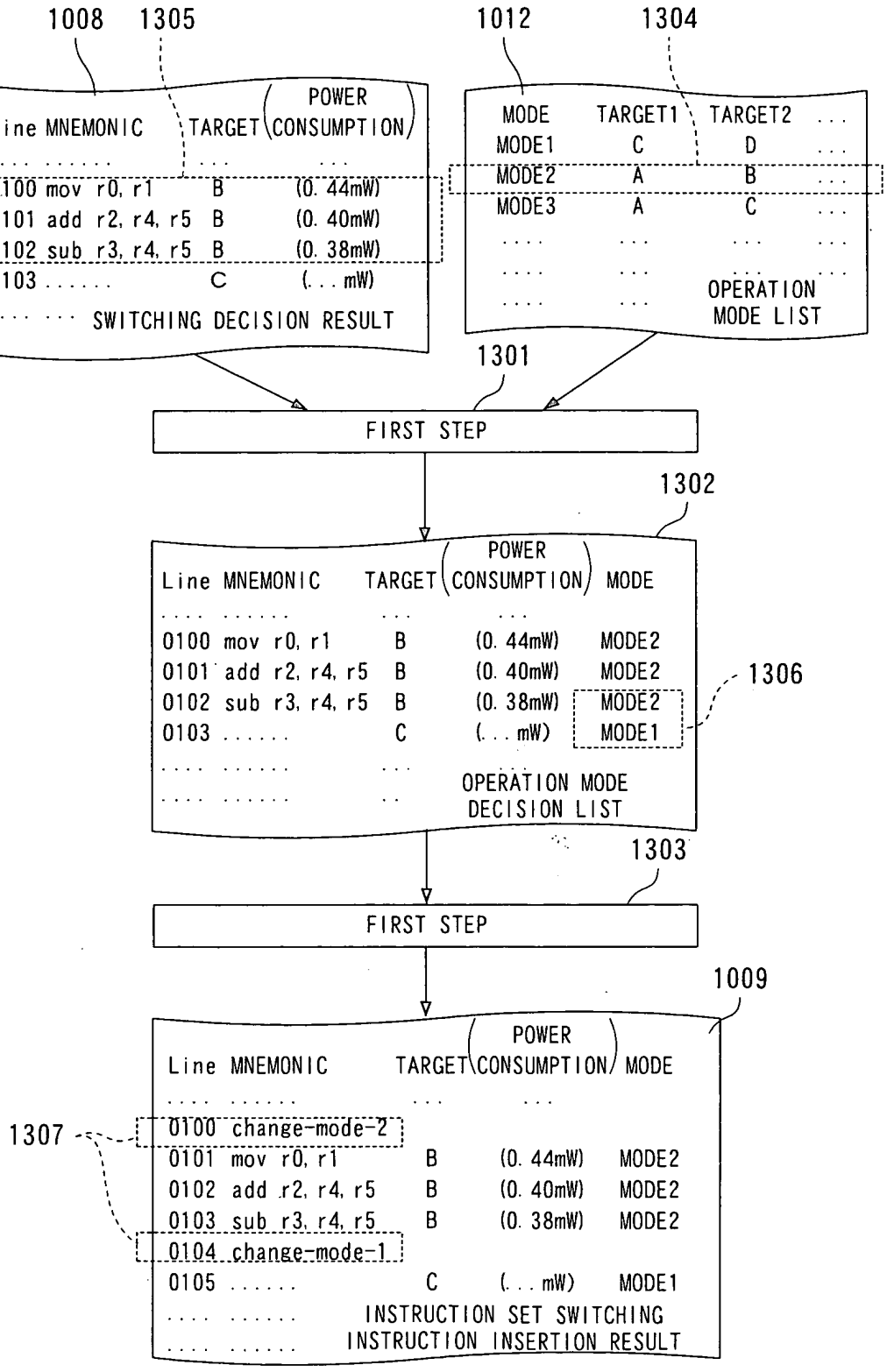
1008
1305
1012
1304
Line MNEMONIC
TARGET
POWER CONSUMPTION
0100 mov r0, r1 B (0.44mW)
0101 add r2, r4, r5 B (0.40mW)
0102 sub r3, r4, r5 B (0.38mW)
0103 ..... C (...mW)
SWITCHING DECISION RESULT
MODE
TARGET1
TARGET2
MODE1 C D
MODE2 A B
MODE3 A C
OPERATION MODE LIST
1301
FIRST STEP
1302
Line MNEMONIC
TARGET
POWER CONSUMPTION
MODE
0100 mov r0, r1 B (0.44mW) MODE2
0101 add r2, r4, r5 B (0.40mW) MODE2
0102 sub r3, r4, r5 B (0.38mW) MODE2
0103 ..... C (...mW) MODE1
1306
OPERATION MODE DECISION LIST
1303
FIRST STEP
1009
1307
Line MNEMONIC
TARGET
POWER CONSUMPTION
MODE
0100 change-mode-2
0101 mov r0, r1 B (0.44mW) MODE2
0102 add r2, r4, r5 B (0.40mW) MODE2
0103 sub r3, r4, r5 B (0.38mW) MODE2
0104 change-mode-1
0105 ..... C (...mW) MODE1
INSTRUCTION SET SWITCHING INSTRUCTION INSERTION RESULT

FIG. 16

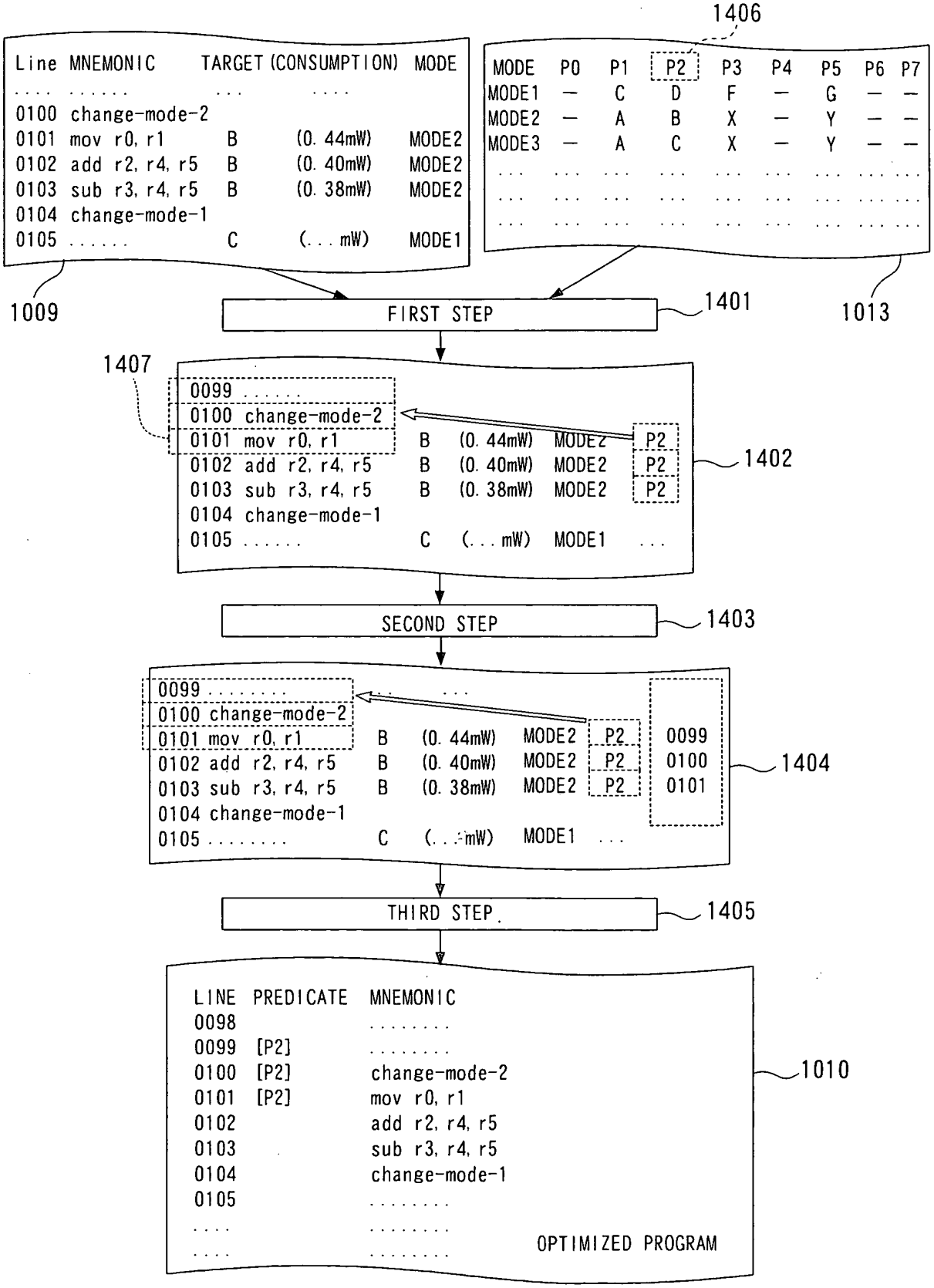
1406
Line MNEMONIC TARGET (CONSUMPTION) MODE
0100 change-mode-2
0101 mov r0, r1 B (0.44mW) MODE2
0102 add r2, r4, r5 B (0.40mW) MODE2
0103 sub r3, r4, r5 B (0.38mW) MODE2
0104 change-mode-1
0105 ..... C (...mW) MODE1
MODE P0 P1 P2 P3 P4 P5 P6 P7
MODE1 — C D F — G — —
MODE2 — A B X — Y — —
MODE3 — A C X — Y — —
1009
1013
FIRST STEP
1401
1407
0099 .....
0100 change-mode-2
0101 mov r0, r1 B (0.44mW) MODE2 P2
0102 add r2, r4, r5 B (0.40mW) MODE2 P2
0103 sub r3, r4, r5 B (0.38mW) MODE2 P2
0104 change-mode-1
0105 ..... C (...mW) MODE1 ...
1402
SECOND STEP
1403
0099 .....
0100 change-mode-2
0101 mov r0, r1 B (0.44mW) MODE2 P2 0099
0102 add r2, r4, r5 B (0.40mW) MODE2 P2 0100
0103 sub r3, r4, r5 B (0.38mW) MODE2 P2 0101
0104 change-mode-1
0105 ..... C (...mW) MODE1 ...
1404
THIRD STEP
1405
LINE PREDICATE MNEMONIC
0098 .....
0099 [P2] .....
0100 [P2] change-mode-2
0101 [P2] mov r0, r1
0102 add r2, r4, r5
0103 sub r3, r4, r5
0104 change-mode-1
0105 .....
.....
.....
OPTIMIZED PROGRAM
1010

FIG. 17

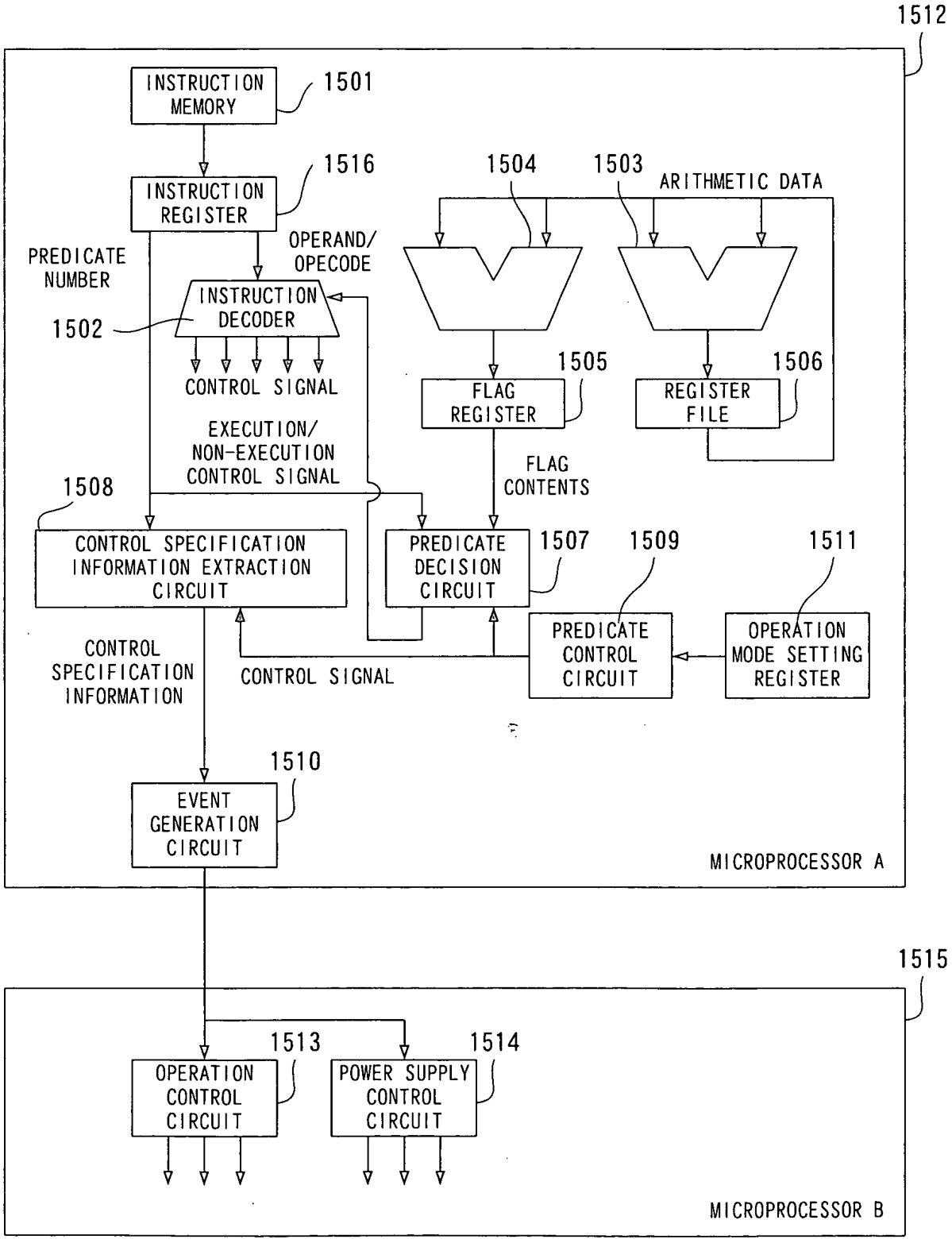
1512
INSTRUCTION MEMORY
1501
INSTRUCTION REGISTER
1516
1504
1503
ARITHMETIC DATA
PREDICATE NUMBER
OPERAND/ OPECODE
INSTRUCTION DECODER
1502
CONTROL SIGNAL
1505
FLAG REGISTER
1506
REGISTER FILE
EXECUTION/ NON-EXECUTION CONTROL SIGNAL
FLAG CONTENTS
1508
CONTROL SPECIFICATION INFORMATION EXTRACTION CIRCUIT
PREDICATE DECISION CIRCUIT
1507
1509
1511
PREDICATE CONTROL CIRCUIT
OPERATION MODE SETTING REGISTER
CONTROL SPECIFICATION INFORMATION
CONTROL SIGNAL
1510
EVENT GENERATION CIRCUIT
MICROPROCESSOR A
1515
1513
1514
OPERATION CONTROL CIRCUIT
POWER SUPPLY CONTROL CIRCUIT
MICROPROCESSOR B

FIG. 18

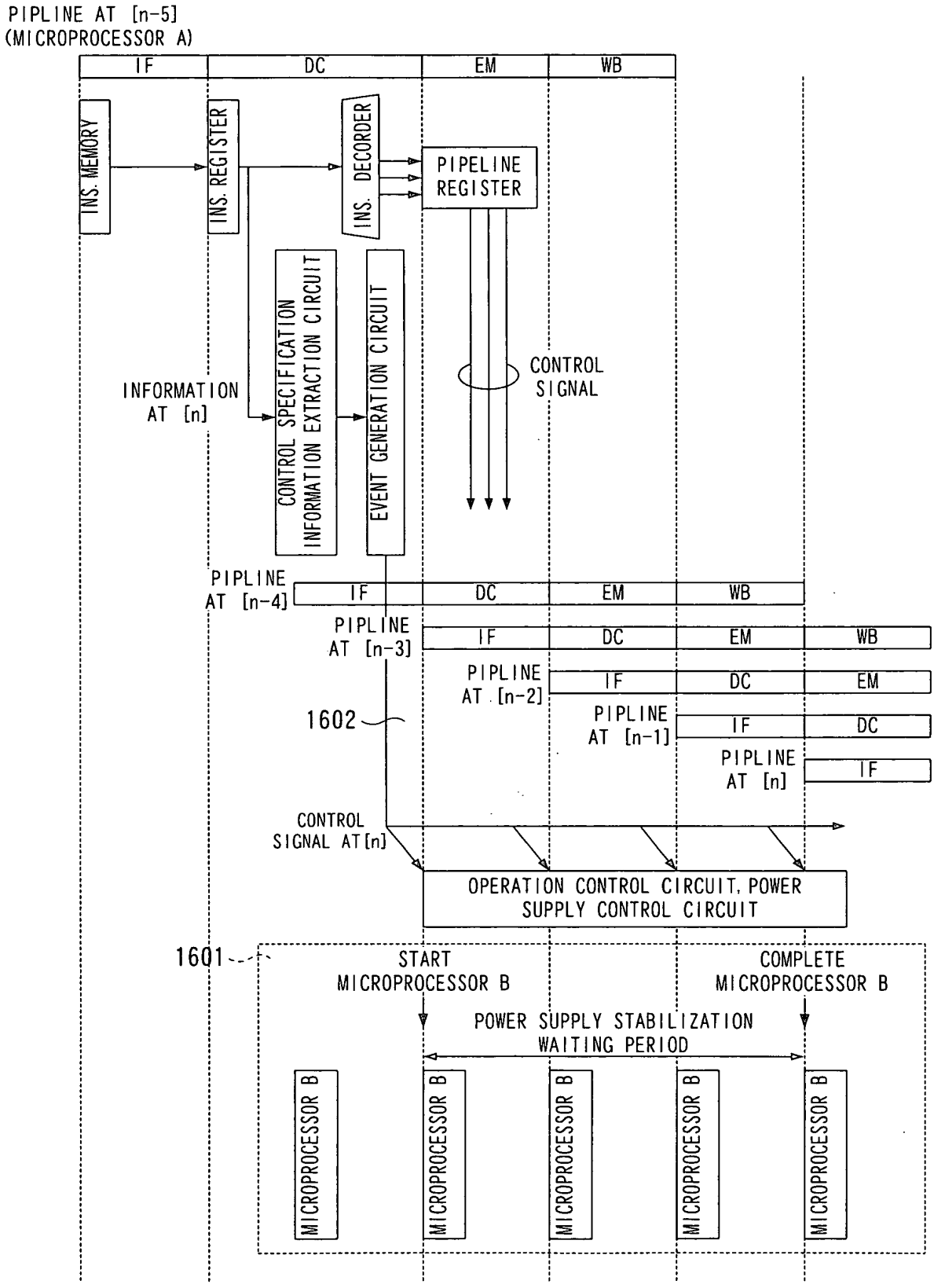
PIPLINE AT [n-5]
(MICROPROCESSOR A)
IF
DC
EM
WB
INS. MEMORY
INS. REGISTER
INS. DECORDER
PIPELINE REGISTER
CONTROL SPECIFICATION INFORMATION EXTRACTION CIRCUIT
EVENT GENERATION CIRCUIT
INFORMATION AT [n]
CONTROL SIGNAL
PIPLINE AT [n-4]
PIPLINE AT [n-3]
PIPLINE AT [n-2]
PIPLINE AT [n-1]
PIPLINE AT [n]
1602
CONTROL SIGNAL AT[n]
OPERATION CONTROL CIRCUIT, POWER SUPPLY CONTROL CIRCUIT
1601
START MICROPROCESSOR B
COMPLETE MICROPROCESSOR B
POWER SUPPLY STABILIZATION WAITING PERIOD
MICROPROCESSOR B

FIG. 19

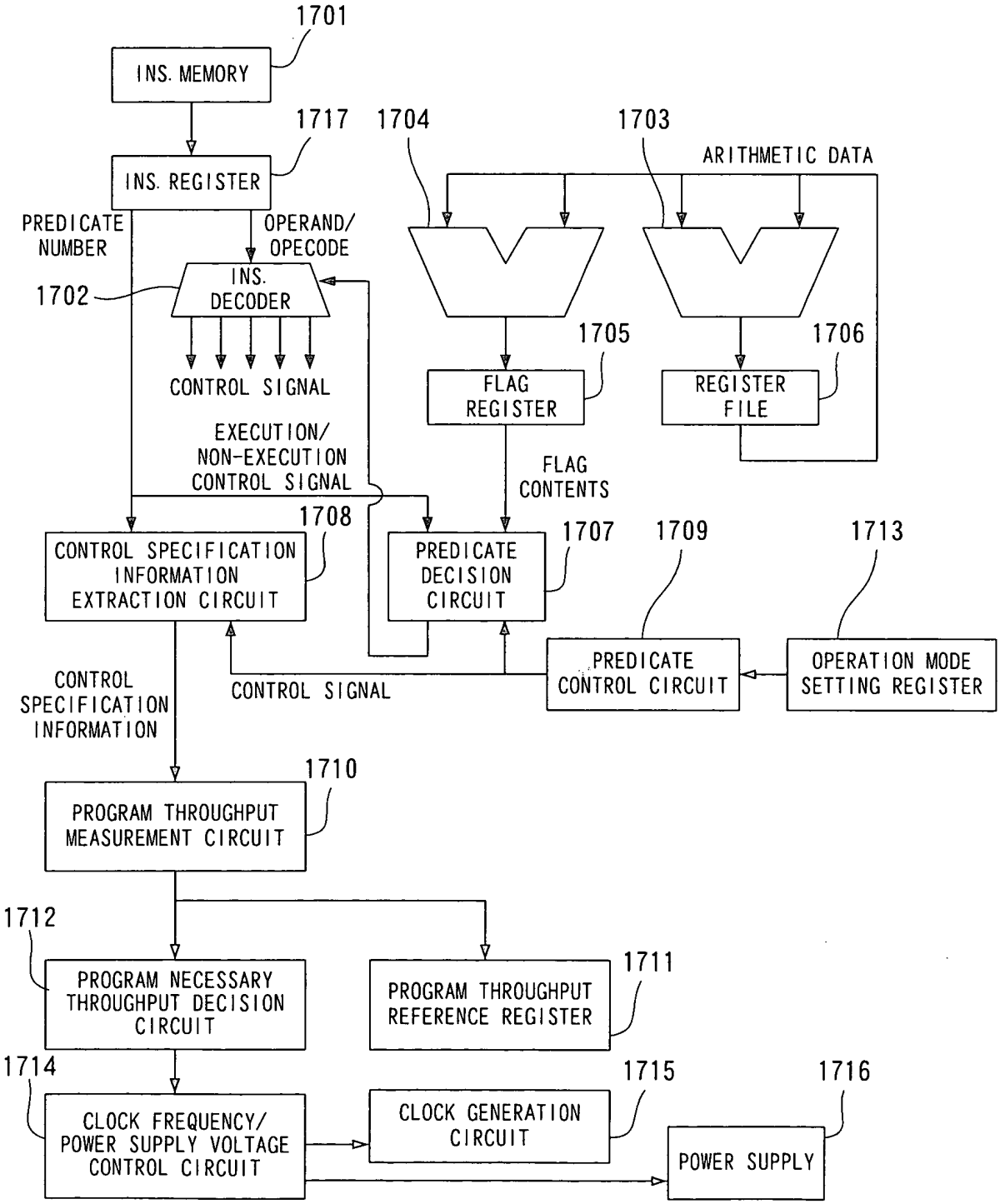
1701
INS. MEMORY
1717
INS. REGISTER
1704
1703
ARITHMETIC DATA
PREDICATE NUMBER
OPERAND/ OPECODE
1702
INS. DECODER
CONTROL SIGNAL
1705
FLAG REGISTER
1706
REGISTER FILE
EXECUTION/ NON-EXECUTION CONTROL SIGNAL
FLAG CONTENTS
1708
CONTROL SPECIFICATION INFORMATION EXTRACTION CIRCUIT
1707
PREDICATE DECISION CIRCUIT
1709
1713
PREDICATE CONTROL CIRCUIT
OPERATION MODE SETTING REGISTER
CONTROL SIGNAL
CONTROL SPECIFICATION INFORMATION
1710
PROGRAM THROUGHPUT MEASUREMENT CIRCUIT
1712
PROGRAM NECESSARY THROUGHPUT DECISION CIRCUIT
1711
PROGRAM THROUGHPUT REFERENCE REGISTER
1714
CLOCK FREQUENCY/ POWER SUPPLY VOLTAGE CONTROL CIRCUIT
1715
CLOCK GENERATION CIRCUIT
1716
POWER SUPPLY

FIG. 20

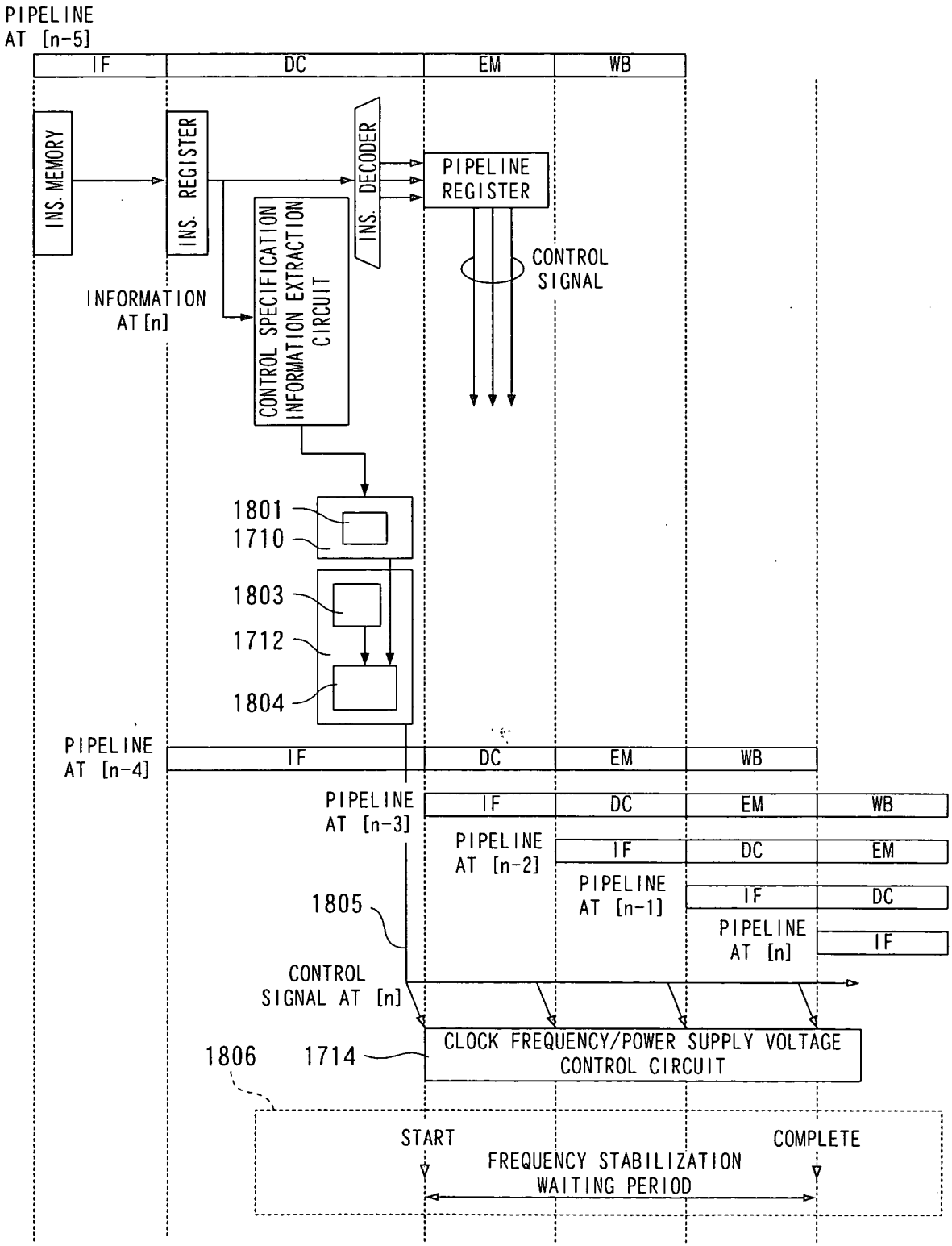
PIPELINE AT [n-5]
IF
DC
EM
WB
INS. MEMORY
INS. REGISTER
INS. DECODER
PIPELINE REGISTER
CONTROL SIGNAL
INFORMATION AT [n]
CONTROL SPECIFICATION INFORMATION EXTRACTION CIRCUIT
1801
1710
1803
1712
1804
PIPELINE AT [n-4]
PIPELINE AT [n-3]
PIPELINE AT [n-2]
PIPELINE AT [n-1]
PIPELINE AT [n]
1805
CONTROL SIGNAL AT [n]
1806
1714
CLOCK FREQUENCY/POWER SUPPLY VOLTAGE CONTROL CIRCUIT
START
COMPLETE
FREQUENCY STABILIZATION WAITING PERIOD

FIG. 21A

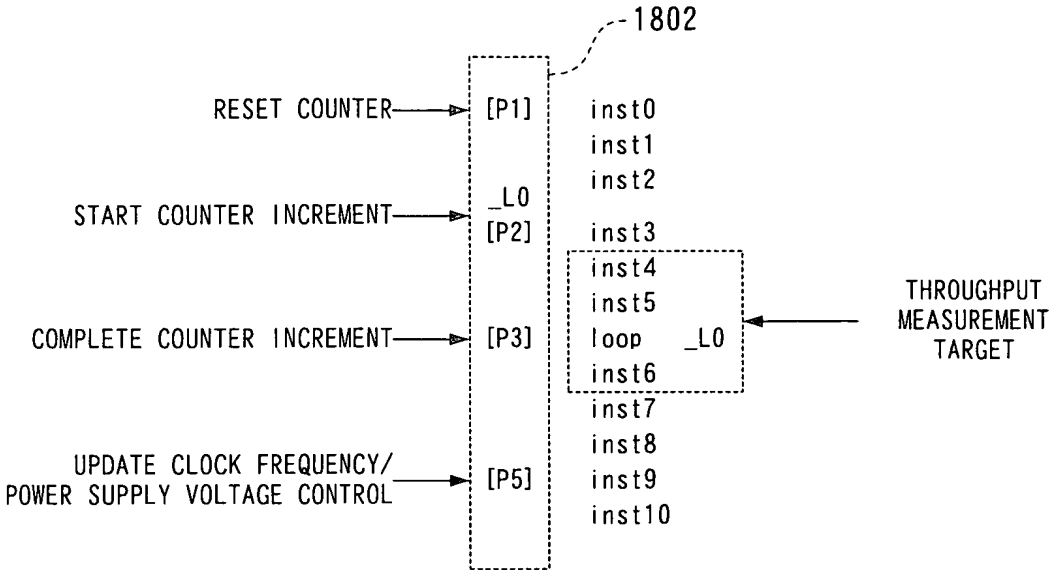

FIG. 21B

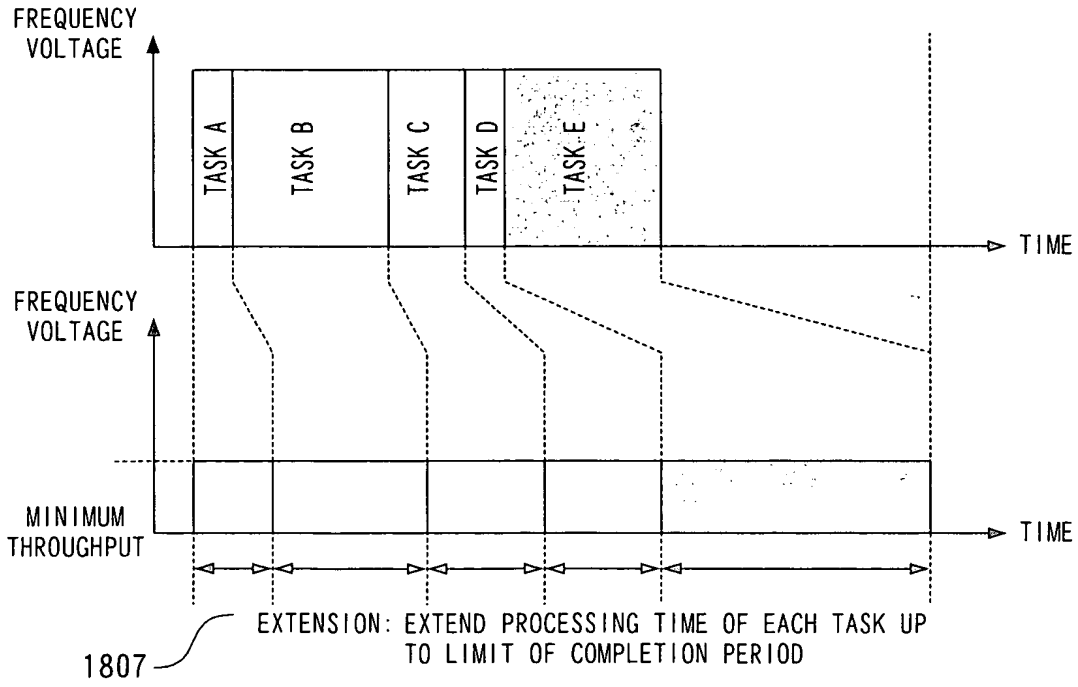

FIG. 22A

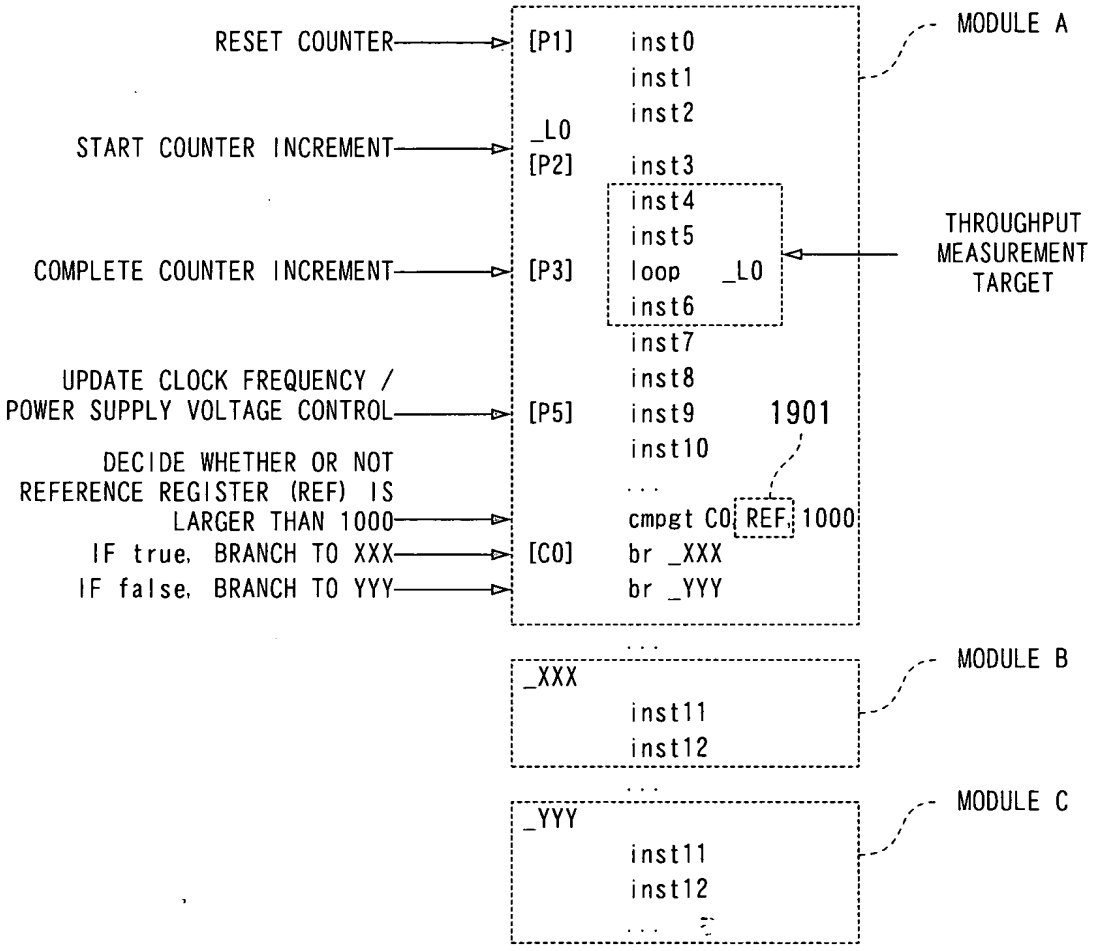

FIG. 22B

PROGRAM HAVING NORMAL PREDICATE		PROGRAM FOR DECIDING THROUGHPUT		
[C0]	inst0	[C0]	inst0	
[C1]	inst1	[P1]	inst1	← THROUGHPUT MEASUREMENT TARGET
[C1]	inst2	[C1]	inst2	
[C2]	inst3	[P2]	inst3	← THROUGHPUT MEASUREMENT TARGET
[C2]	inst4	[P2]	inst4	← THROUGHPUT MEASUREMENT TARGET
[C0]	inst5	[P0]	inst5	← THROUGHPUT MEASUREMENT TARGET
[C0]	inst6	[P0]	inst6	← THROUGHPUT MEASUREMENT TARGET
[C3]	inst7	[C3]	inst7	
[C3]	inst8	[P3]	inst8	← THROUGHPUT MEASUREMENT TARGET
[C5]	inst9	[P5]	inst9	← THROUGHPUT MEASUREMENT TARGET
[C5]	inst10	[C5]	inst10	